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AUTO-CONFIGURED LIN BUS NODES

The invention relates to electronic devices and more specifically to electronic devices used within systems conforming to the LIN Bus standard.

LIN Bus is a name given to an open protocol defined for use in communicating between a number of distributed modules. Many applications of the LIN Bus are targeted specifically at the automotive industry.

In LIN Bus applications each module contains an interface circuit, usually implemented as a single integrated circuit, which interfaces to the common signal conductor or BUS and handles the protocols associated with the messages and the required responses.

Each module in a system has a unique identity, ID, within the system, which enables a bus master to communicate with a selected module or a group of modules within the system.

As originally defined, all the modules within a LIN Bus system are connected in parallel. That is they share a BUS across which all messages and communications are sent and received. Each module has a pull up resistor and an active pull down transistor. Message initiation is asynchronous and message collisions are resolved by arbitration means. Since a pull down or active state, will take precedence over a pull up, or recessive state, any transmitting module seeing an active state when transmitting a recessive state knows that another module is transmitting. Under such circumstances the module transmitting the active state takes precedence and any other modules must cede the bus and try again later.

Each module is assumed to be preconfigured before installation with its own unique ID.

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Such an assumption places demands on the manufacturers, installers and most particularly on those repairing a system to correctly configure every module before installation. An extension to the system protocol providing a method of configuring a module with an ID after installation was thereby proposed and implemented by Bosch  
5 and Philips amongst others and has been favorably received.

In such a system the electronic interface between the BUS and the modules is altered. In particular, the system incorporates extended capability modules capable of being configured wherein each extended capability module has two connections to the BUS, the normal modules having only one connection to the BUS.

10 The BUS is made discontinuous at each extended capability module and one connection is made to each side of the discontinuity. Extended capability modules are thus connected in a daisy chain configuration whilst normal modules are connected to the BUS as before. The extended capability modules maintain signal continuity along the BUS but introduce a nominal (approximately one ohm) series resistance per  
15 extended capability module.

Extended capability modules are manufactured in a non configured state but can be configured after installation. In a non configured state a module has no identification (ID) and cannot be selectively communicated with. To overcome this limitation, all un-configured extended capability modules respond to a configuration  
20 request message transmitted onto the BUS by a bus master, by turning off their pull down transistors and forcing a current through their pull up transistor onto the common signal conductor. These forced currents will flow along the common signal conductor to the bus master which has its pull down transistor turned on. By this means every un-configured extended capability module except one will see a voltage

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across the nominal one ohm series resistance introduced at each extended capability module. The exception is the module furthest from the master as defined by the daisy chaining connections. This un-configured extended capability module is thus uniquely identified and enables itself for programming of an ID within the system.

- 5 The procedure can be repeated until all un-configured extended capability modules are configured with an ID.

This scheme has a number of limitations. The normal performance of the bus is degraded by the introduction of the series resistances. The series resistance within an extended capability module is normally implemented within an integrated circuit  
10 and the tolerance of such resistors is wide. The forced currents are all sunk via the bus master, which has maximum current capabilities and a current limiting capability defined within the specification. The value of the forced current used to identify and enable one module for configuration must be small and carefully selected and controlled. The voltages developed across the series reset or within a module are also  
15 small and must be measured with high accuracy.

A better solution would deliver the benefits of simple selection of one of a number of an un-configured extended capability module for configuration whilst imposing fewer restraints on the tolerances of individual elements within the system and maintain compatibility with the LIN bus specification.

- 20 It is thus an object of the invention to provide an improved scheme for configuring modules that is compatible with the LIN BUS standard.

According to a first aspect of the present invention there is provided a reconfigurable module having means for being configured with an ID and also having

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embedded within it at the manufacturing stage a fixed unique Chip Identification Code (CIN) for use during a configuring operation.

Preferably, said module is a module compatible with the LIN Bus Standard. Preferably, said module has two LIN Bus interface pins connected by a series resistor.

5 Preferably the series resistor is a 1 ohm or similar value resistor. In this manner the modules may be connected as a daisy chain of slave nodes on the LIN Bus.

Preferably said module further comprises a pull up resistor and a pull up current source for forcing a pull up current through the pull up resistor.

Preferably if a number of said modules are connected in a daisy chain manner  
10 standard LIN Bus arbitration rules apply for selecting one module from the daisy chain. Preferably said pull up current only flows whilst said module is selected.

Preferably said module further comprises a position counter, which may be incremented to indicate the position of the module in a daisy chain.

In an alternative embodiment said module further comprises a random code  
15 generator for generating a random code of a plurality of bits in length to identify the module as an alternative to the CIN code. The number of bits in the code is chosen to minimize the possibility of two modules having the same random code.

According to a second aspect of the present invention there is provided a LIN  
bus system comprising a plurality of modules linked to a LIN bus along which  
20 electronic data or instructions can be sent to and from each said module, at least one of said modules being non configured and having no unique identification address associated therewith, said at least one module having a unique code associated therewith, said system further including configuration means which interrogates said modules and detects the unique code of said at least one non-configured module and

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transmits a configuration signal to the module to configure the module, each said non configured module including counter means which is incremented each time a non configured is configured, said counter of each non-configured module, once configured, providing a unique code which is indicative of the position of the module  
5 in the system.

Preferably the at least one module having a unique code associated therewith is a reconfigurable module according to the first aspect of the invention and said unique code may be either a CIN or a randomly generated code or any other suitable unique code.

10 Preferably if such a LIN Bus system comprises a plurality of non-configured reconfigurable modules said non-configured reconfigurable modules are connected together in a daisy chain manner. Additionally and preferably a configuration sequence is performed to configure each of the plurality of non-configured reconfigurable modules. During a configuration sequence the bus master transmits a  
15 configuration request and all non-configured reconfigurable modules respond by transmitting a reply consisting of their unique code. Preferably, standard LIN bus arbitration rules apply, wherein active states win over recessive states, and one non-configured reconfigurable module will thus win the arbitration and become the 'selected module'.

20 Preferably the selected module then forces a current through its pull up resistor. Non-selected non-configured reconfigurable modules can monitor this current through their series resistors and thereby determine that a selected module is responding.

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Preferably, each non-configured reconfigurable module incorporates a position counter incremented on each occasion that a selected module responds with a forced current. The position counter on a particular non-configured reconfigurable module is however not incremented when the particular non-configured reconfigurable module is itself selected. Additionally the position counter on a particular non-configured reconfigurable module is not incremented after the particular module has been selected. In this manner as each module in the daisy chain is selected in turn, each module has its position counter fixed showing its position in the daisy chain. Once all un-configured extended capability modules have been selected each will have a position counter showing a unique position for that module within the daisy chain. This unique position counter value can then be used to select a module and configure it for use in the system.

The benefits of such an improved system are that only one module is forcing current at a time thus simplifying the task of determining that a current is flowing by reducing the accuracy required for the measurement. The tolerances of the components are also less onerous.

According to a third aspect of the present invention there is provided a method of configuring a LIN Bus system according to the second aspect of the present invention comprising a plurality of said non-configured reconfigurable modules connected in a daisy chain manner comprising the steps of: transmitting a configuration request from a bus master; selecting one module from the daisy chain by standard LIN bus arbitration rules; forcing a current through the pull up resistor of the selected module; incrementing the position counter of each module within the daisy chain that is not currently or previously selected; repeating the above steps until

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each module in the daisy chain has been selected, the position counters for each module thus showing its unique position in the chain; and using the unique position counter value to select and configure a desired module or a plurality of desired modules.

5           In order that the invention be more clearly understood, one embodiment will now be described further herein and with reference to the accompanying drawings in which:-

- Figure 1       is a block diagram of a reconfigurable module according to the present invention showing its interface with a series resistance;
- 10       Figure 2       shows a plurality of such reconfigurable modules connected to a common signal line; and
- Figure 3       illustrates how the position of each module within the daisy chain is determined.

Referring now to figure 1 the module comprises a normal LIN bus interface  
15   pin spilt into a LIN\_H pin, 101, and a LIN\_L pin, 102, connected with a resistor Rac, 103, of typically 1 ohm. This enables modules to be connected as a daisy chain of slave nodes on the LIN bus. The module further comprises a pull up resistor 104 and a pull up current source Iac, 105, which can be activated during auto-configuration. During normal communication this current source is always off and has therefore no  
20   influence. This current source has a typical value of 8mA.

During the auto-configuration procedure the voltage across the resistor Rac is monitored by amplifier means, 107. The LIN pull up resistor, 104, can also be switched off during the auto-configuration process.

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Figure 2 shows an example of a daisy-chained LIN bus for auto-configuration. The master module, 201, is located at one end of the bus. The modules 1 to n, 211, ..., 21n, are slave nodes with auto-configuration capability. The modules are daisy-chained by connecting the LIN\_H pin, 101, on one module to the LIN\_L pin, 102, on an adjacent module, in the case shown in figure 2, the module adjacent and to the right.

Modules n+1, ... are standard slave modules not reconfigurable modules according to the invention and as such they can be connected anywhere on the LIN bus. There may be any desired combination of reconfigurable slave modules and standard slaves connected to the bus, including slaves connected in a tree structure as long as the reconfigurable slave modules are connected in a daisy chain.

The reconfigurable modules can have following auto-configuration states:

- Unaddressed: the node is not identified (i.e. the node has not assigned an ID and can thus not be assessed for normal messages requiring the ID of a node).
- 15     • Selected: the node has been selected during the on-going auto-configuration interrogation message. It will switch to the addressed state at the end of the message.
- Addressed: the node has been addressed during the auto-configuration procedure. It is waiting the end of the auto-configuration procedure to get assigned his node ID.
- 20     • Identified: the node has received his proper ID (which is written in eeprom) and can be accessed for all application messages.

A module that has never been identified has ID=0 written in non-volatile memory NVM, such a module will enter the unaddressed state after power



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on/reset. Additionally, a module that is not in the identified state will enter the unaddressed state after power on/reset.

The module has a unique chip identification number (CIN) code built in at manufacture. This code can be any code, except a code consisting of all zeros. In practice this code consists of data defining batch No., wafer No and die position on the wafer. Typically the CIN has a total of 48 bits (6 bytes) of unique code.

No special hardware is required for the master. Any micro-processor equipped with a regular full duplex Uart, associated with a standard Lin physical interface circuit (such as the TH8082 available from Melexis) can be used. The software running on the master must be able to send the frame items (Uart bytes) in a different way than for the regular frames.

The auto-configuration system makes use of the user defined extended frame message (Id 0x3E). The advantages of this use of the extended frame message are that it leaves the regular LIN identifiers untouched and available, the number of bytes is free and can thus be optimized for each message, and the byte containing the error flag can be located at the end of the frame, after the checksum (to allow for signaling of checksum errors, by the master as well as the slaves).

The first byte of the extended frame message is sent by the master and identifies one of the configuration frames shown in the table below (the following bytes depend on the function).

<b>Id</b>	<b>First Byte</b>	<b>Function</b>	<b>Following bytes</b>	<b>Last bytes</b>
<b>0x3E</b>	<b>1111 1111</b>	<b>UAD</b>	<b>2 data bytes</b>	<b>Checksum</b>

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<b>0x3E</b>	<b>1111 1110</b>	<b>INT</b>	<b>CIN</b>	<b>Checksum &amp; Flags</b>
<b>0x3E</b>	<b>1111 1101</b>	<b>IDS</b>	<b>ECU address byte</b>	<b>Checksum &amp; Flags</b>
<b>0x3E</b>	<b>1111 1100</b>	<b>FRQ</b>	<b>various</b>	<b>Check sum</b>
<b>0x3E</b>	<b>1111 0---</b>	<b>Reserved for future use</b>		

Some aspects of the table are discussed in more detail below.

UAD: un-address all auto-configuration slaves, the UAD message is a regular message with data sent by the master. When the master initiates the UAD command all auto-configuration slaves reset their node identifier ID to 0 and set their internal position counter to 1. The result is that all slaves are now in the unaddressed state and the bus is consequently ready to start the auto configuration process.

INT: interrogates all auto-configuration slaves, the INT message is an extended message containing 8 bytes of data. When the master initiates this command, it is processed by all auto configuration slaves who are in the unaddressed or addressed state. During the first 6 bytes (Data 0-5), all unaddressed slaves send their CIN code in an order defined by arbitration: if a slave detects a dominant level while trying to transmit a recessive level, it loses the arbitration and switches to a recessive level for the remaining of the CIN code transmission. During these bytes the master must send a data byte 0xFF (all recessive) to initiate the arbitration.

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At the end of the CIN code transmission one slave only will have succeeded in transmitting its full CIN code and therefore recognizes itself as selected. This slave will transmit the checksum to result in a correct message for all standard slaves. This selected slave will switch to the addressed state at the  
5 end of the message (if the checksum transmission and the error flag are correct).

During the next byte (Data 6), the master sends 8 dominant bits, while all auto-configuration slaves switch off their LIN pull up resistor: - During the first bits all auto-configuration slaves in the unaddressed state will calibrate on the bus. This means that the voltage across the resistor  $R_{ac}$  is amplified and measured by  
10 an ADC. This will be used as a reference voltage during the next 4 bits. During the second 4 bits the selected slave will enable its current source  $I_{ac}$  and all addressed and unaddressed slaves will monitor the voltage drop across their resistor  $R_{ac}$ . If the voltage threshold is exceeded (i.e. the chip detects a current  $I_{ac}$ ), the slave will increment its position counter.

15 During the last Byte (Data 7) all unaddressed slaves send a dominant bit followed by a recessive bit (the addressed slaves and the selected slave do nothing). The master also sends a 0xFFbyte to initiate the response from the slaves. This is the 'More' flag. It indicates that at least 1 slave is still in the unaddressed state. The remaining 6 bits can be used to signal an error flag (a  
20 slave disagreeing with the configuration sequence sends 1 dominant bit followed by 5 recessive bits).

The message is completed by the selected slave sending the checksum. In case no slave responds (CIN is fully recessive), the master must send the corresponding checksum to still have a correct message. At the end of the

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message the selected slave switches to the addressed state if no error has been flagged. If an error has been flagged the slave switches back to the unaddressed state.

5       The master repeats the interrogation message until all the reconfigurable slaves are in the addressed state i.e. until the 'More' flag is not returned. The master determines that this is completed correctly if: all checksums were correct; no 'all recessive CIN code' was received; no error flag was received; and the 'More' flag was transmitted correctly (for all messages but the last one.)

10       Figure 3 illustrates how the INT sequence works. The bus connects a master node with five reconfigurable slave nodes 1-3, 6, 7 and three standard slave nodes 4, 5, 8. Each of the reconfigurable slave nodes is selected in turn. In the example the order is 2, 3, 7, 1, 6. The nodes are selected in order of their CIN codes. The resulting values shown in each position counter after each cycle of the INT sequence is shown. When the configuration process is completed, the internal  
15       counter Position counter (PosCnt) of each slave contains its position in the daisy chain. This value, the ECU address, is be used to configure the modules to suit the application.

20       IDS: identifies an auto configuration slave, used to configure the node according to function on the bus, it transfers a module from the addressed state to the identified state. During this message the master accesses a slave according to the value stored in the position counter (the ECU address), to give the node an ID value which is typically stored in eeprom. In order that more than one identifier may be specified for each slave, a function code is used to select the identifier to be set.

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FRQ: function request, allows interrogation of a slave based on its ECU address. It can be used after the INT sequence but before the IDS message to verify and or identify the function of the particular module.

5 In an alternative embodiment the CIN code (which is stored in eeprom) can also be replaced by a random generated code of x bits. In such embodiments, a random code generator is incorporated into the module. The right value for x is calculated to minimize the risk of different modules within the daisy chain having identical codes.

10 If however the situation should arise that two modules have identical codes, this can be overcome. If two slaves have identical codes, both will be selected simultaneously and they will both activate their current source. There are two alternatives by which this can be dealt with. Firstly, the selected slave closest to the master will detect a current flowing through its resistor and therefore will recognize that it is not the only slave selected and will consequently react as if not  
15 selected. Secondly and alternatively, an error flag can be generated either by the master or by the selected slave closest to the master which consequently restarts the procedure. The advantage of this embodiment is that there is no need for non volatile memory to be incorporated into the module and thus the configuration sequence can be run on each power on/reset.

20 It is of course to be understood that the invention is not intended to be restricted to the details of the above embodiments which is described by way of example only.